REMARKS

The Office Action mailed November 25, 2002 has been reviewed and carefully considered. Claims 1-11 are pending, of which claim 1 is the independent claims. Claim 1 has been amended. Reconsideration of the above-identified application, as herein amended and in view of the following remarks, is respectfully requested.

Claims 1-11 were rejected under 35 U.S.C. 112, second paragraph, as indefinite due to the base claim 1 recitation that "a layer comprising silicon carbide is applied as the etch stop layer (12)." Based claim 1 has been rephrased for clarity to recite that the etch stop layer (12) comprises silicon carbide. The amendment of claim 1 is believed to overcome the rejection.

Claims 1-11 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 5,880,018 to Boeck et al. ("Boeck") in view of U.S. Patent No. 6,159,845 to Yew ("Yew").

The invention as recited in claim 1 features the step of "etching a via (14,15,16) in the dielectric layer (13) over the conductor (3,4,5), and stopping on the etch stop layer (12) . . ."

Discussion of the stopping step, in the inventive method, is found in the specification from page 5, line 19 to page 6, line 5.

Boeck, by contrast, mentions conventional (col. 7, lines 36(37)-37(38): "Conventional") techniques, but fails to disclose or suggest a stopping step as explicitly required by the language of claim 1. See, for example, Boeck, col. 7, line 36(37) to line 41(42).

Yew reveals a semiconductor device that is etched, but likewise fails to disclose or suggest a stopping step as in the invention of claim 1.

The proposed Boeck/Yew combination would thus fail to feature the stopping step explicitly required by the language of claim 1, which is therefore believed to be patentable over the applied references, alone or in combination, for at least this reason.

Reconsideration and withdrawal of the rejection is respectfully requested.

As to claims 2-11, they depend from and thus include all the limitations of base claim 1, and are likewise deemed to be patentable for the same reason.

In view of the foregoing amendments and remarks, it is believed that this application is now in condition for allowance. The Examiner is invited to contact the undersigned in the event of any perceived outstanding issues so that passage of the case to issue can be effected without the need for a further Office Action.

Respectfully submitted,

Aaron Waxler
Registration No. 48,027

Date: 2/24/03

By: Steve Cha
Attorney for Applicant
Registration No. 44,069

Mail all correspondence to:
Aaron Waxler, Registration No. 48,027
US PHILIPS CORPORATION
580 White Plains Road
Tarrytown, NY 10591
Phone: (914) 333-9608
Fax: (914) 332-0615

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Steve Cha, Reg. No. 44,069
(Name of Registered Rep.)

2/24/03
(Signature and Date)

VERSION WITH MARKINGS SHOWING CHANGES

IN THE CLAIMS:

Amend claim 1 as follows:

1. (Amended) A method of manufacturing an electronic device, a semiconductor device in particular but not exclusively, which method comprises the steps of:

_____-applying a semiconductor substrate (1) which is provided with a conductor (3,4,5) at a surface (2), the conductor (3,4,5) having a top surface portion (6) and sidewall portions (7), of which at least the top surface portion (6) is provided with an etch stop layer (12) comprising silicon carbide;~~,~~

_____-applying a dielectric layer (13);~~,~~

_____-etching a via (14,15,16) in the dielectric layer (13) over the conductor (3,4,5), and stopping on the etch stop layer (12) to create an exposed part of the etch stop layer (12);~~,~~

_____-removing the exposed part of the etch stop layer (12) inside the via (14,15,16) from at least the top surface portion (6) of the conductor (3,4,5); and~~,~~

_____-filling the via (14,15,16) with a conductive material (18)~~-characterized in that a layer comprising silicon carbide is applied as the etch stop layer (12)~~.